IMPROVED ELEMENTARY CELL GaAs POWER FET STRUCTURE *

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ABSTRACT

An improved design for the elementary cell of X-band power GaAs FETs is described. It includes : a buffer layer, a graded doping profile, an offset recessed gate structure, a multifinger high density gate structure and via holes. Furthermore, three different types of source interconnections for the interdigitated cell will be compared.

Introduction

There have been many papers published concerning power GaAs FET devices. A number of improvements have been introduced over the last few years in order to increase simultaneously the maximum available output power and the associated gain at higher and higher frequencies.

Important factors contributing to high gain and power level include the use of a buffer layer, an active layer with a graded profile, an offset recessed gate structure, multifinger high density gate structure and via holes. Furthermore, reliability is noticeably improved if ohmic contacts are made of Ge Au Ni , if aluminium is employed for the metal gate, if all the pads are overlayered with TiPtAu and finally if the active zones are protected by SiO_2.

A number of laboratories have achieved excellent performances but none of them, to our knowledge, have taken advantage simultaneously of all these factors. We have therefore designed an improved structure for the elementary cell of a power FET gathering the above mentioned features required for high power gain and reliability. This paper will discuss the factors contributing to the high gain and output power performance. After a description of the fabrication process, we will compare the advantages and disadvantages of 3 types of second level source interconnection, over the metal gate, over the channel and over the drain all made on the same epitaxial layer.

Technical discussion

Device

Fig. 1 shows the mask layout of the structure proposed in this work. Basically it consists of 6 gate fingers of nominally 1 x 100 µm each, located

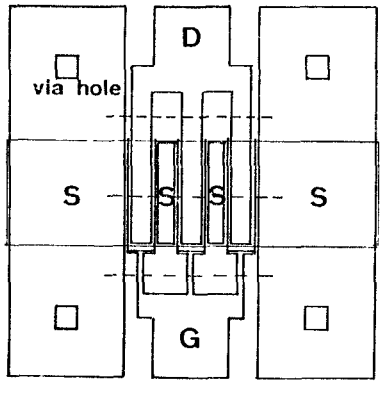

Fig. 1 : mask layout of the FET structure

in a drain source spacing of 5 µm, the gate source spacing being about 1.5 µm. The choice of a 600 µm total gate width has been retained because in a 50 Ω system, the VSWR is minimized in X-band, thus facilitating microwave measurements.

The active layer ($\sim$ 0,7 µm, $\sim$1.2 10^{17}) is grown by vapor phase epitaxy on Cr-doped substrates using the $Ga/AsCl_3/H_2$ growth system. A high resistivity buffer layer (2-3 µm) non-intentionally doped is grown before the growth of the active layer.

The introduction of a high resistivity buffer layer between the substrate and the active layer improves the quality of the interface as far as mobility and traps are concerned and reduces parasitic effects such as looping, bumping and premature avalanche effects due to the high electric field appearing in this region.

The first step of the fabrication process is to isolate the active zone by a mesa technique followed by a boron implantation. This technique is used in order not to have a mesa step higher than 0.4 µm, thus avoiding technological problems when the gate passes over the mesa edge. In the second step, the ohmic contacts are formed by a lift off method using the undercutting of a photoresist (1) ; they are made of AuGe eutetic ($\sim$ 2000 Å) covered with a thin Ni layer : this sort of contact leads to good contact resistances compared with other alloys. In addition, it minimizes electromigration phenomena by reducing the grain size of the alloyed contact thus achieving a better reliability. The alloying is formed at about 450°C for a short time. The third step consists of defining the gate pattern in a photoresist. The position of the gate is nearer to the source than to the drain in order to increase the gate breakdown voltage (2) thus permitting a larger swing voltage and therefore improving the power performance. In order to increase the drain to source breakdown voltage and to achieve the best output power, the active layer is chemically etched through the gate pattern until the layer under the gate is equal to the optimum thickness for power (3). This is obtained by controlling the current flowing through the channel. This technique increases the drain to source breakdown voltage by diminishing the drain current density and therefore the high electric field region near the drain edge responsible for the breakdown in a planar device. After metallization and lift off of the metal gate (Al) all the device is covered by a 1 µm thick SiO_2 layer. This thickness represents a good compromise to lower parasitic interconnection capacitances. Photoresist is then deposited and all the contact pads are opened through the SiO_2, the overhang resulting from the undercutting of SiO_2 is used to lift a multilayer formed by a titanium layer and by platinum layer evaporated on top. A last level of 0.25 µm thick lifted TiAu ensures the interconnection of elementary sources, this sort of multilayered contact is well known for its high reliability in bipolar transistors. In addition the electromigration phenomena are reduced because the presence of SiO_2 on all the active areas prevents the formation of lumps generally associated with electromigration. Three types of source interconnection have been made. In a first type, a metal strip joins the different sources by passing over the gate between the gate pad and the gate fingers ; in the second type, the metal strip passes over the middle of the active channel and in the third type,

* This work is partly supported by DRET

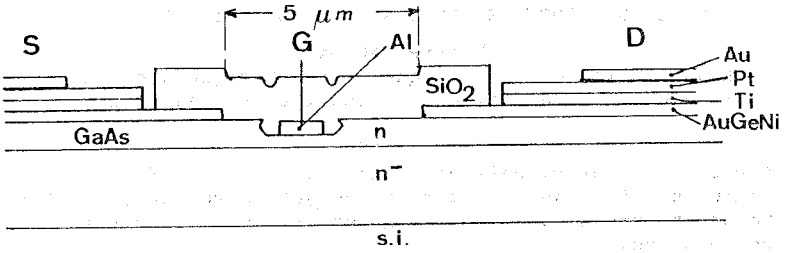

Fig. 2 : cross-section of an elementary FET

the metal strip passes over the drain between the drain pad and the drain fingers. Lastly the total thickness of the substrate is reduced to 50 µm for good thermal resistance and to enable via holes to be made and then the reverse side of the chip is metallized. Fig. 2 shows a cross-section of an elementary FET.

Performance

Fig. 3 shows the d.c. characteristics of the 600 µm gate width cell. As can be seen, the transconductance is in excess of 100 mA/V mm gate width and saturation voltage is low (1.5 V) compared with the dimensions of the channel. No difference in terms of current and voltage between the three types of interconnection has been observed. The small signal S parameters of the three types of devices have been analyzed on an automatic network analyzer between 2 and 12 GHz. S_{11} and S_{22} are represented in fig. 4 and Table 1. For this purpose, the devices were inserted on a 50 Ω coplanar microstrip line 4 mm long (without heatsink and biased at V_{DS} = 6 V and $I_{DSS}/2$). Associated gains have been calculated and are shown in fig. 5.

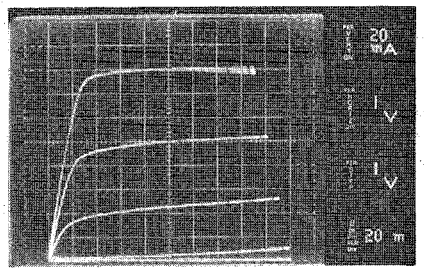

Fig. 3 : I-V characteristics of the 600 µm gate width cell.

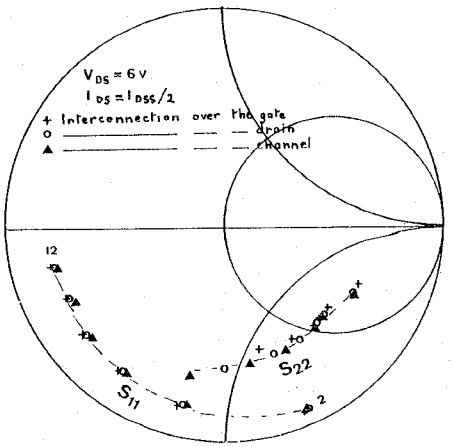

Fig. 4 : Input and output S parameters from 2 to 12 GHz.

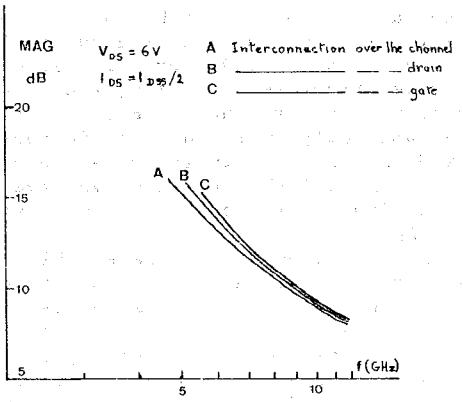

Fig. 5 : Gain performance versus frequency obtained from S parameters measurements

At 12 GHz, the MAG is in excess of 8 dB. In terms of S_{11}, S_{12}, S_{22} no noticeable difference is observed between the three structures and the slight difference can be attributed to the electrical dispersion of the chip carrier and to the incertitude of measurements.

The only difference results from S_{22} which are slightly different especially at low frequencies. In terms of gain, source interconnection over the gate is slightly better than the one over the drain which in turn is slightly better than the one over the channel.

For output power measurements devices were mounted in a water-cooled power FET package . At 12 GHz with V_{DS} = 10 V and $I_{DS} = I_{DSS}/2$, an output power in excess of .5 W/mm gate width has been achieved with an associated gain of 7 dB for the interconnection over the gate, this represents about .5 - .8 dB better in gain than the 2 other types of interconnection which have presented similar output power performance.

Conclusion

An improved elementary cell GaAs FET structure has been made which is simultaneously capable of both high gain and high power at 12 GHz. The structure with source pads connected down to the ground facilitates the associations of a large number of elementary cells in a line configuration.

We have evidence that an interconnection over the gate is better than the interconnection over the drain or over the channel. Because of its technology, it is believed that reliability has been improved without loss of performance.

V_{DS}=6V, $I_{DS}=I_{DSS}/2$	interconnection over the gate				interconnection over the drain				interconnection over the channel			
f (GHz)	S_{11}		S_{22}		S_{11}		S_{22}		S_{11}		S_{22}	
	ρ (dB)	φ (°)	ρ	φ	ρ	φ	ρ	φ	ρ	φ	ρ	φ
2	- .8	- 67	-3.62	-24	- .82	- 65	-3.58	-28	- .87	- 65	-3.52	- 28
4	-1.54	-105	-4.54	-37	-1.63	-103	-4.32	-44	-1.7	-102	-4.31	- 47
6	-1.83	-127	-4.41	-41	-1.94	-125	-4.06	-51	-2.05	-123	-4.1	- 56
8	-1.97	-143	-4.12	-48	-2.08	-143	-3.65	-59	-2.25	-140	-3.63	- 67
10	-2.22	-156	-4.4	-60	-2.34	-154	-3.72	-73	-2.52	-153	-3.5	- 84
12	-1.97	-167	-4.76	-75	-2.09	-165	-3.71	-90	-2.28	-166	-3.09	-104

TABLE 1 : Comparison between input and output S parameters for the three types of interconnection

Acknowledgments

The author would like to thank J. Bellaiche for his contribution in FET processing and M. Parisot for the small signal S parameters measurements. He also thanks L. Hollan and J.P. Chané for supplying material.

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